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PAN1321-SPP

Infineon's
BlueMoonUniversal Platform

Wireless Modules

User's Manual

Hardware Description
Revision 3.0

Panasonic
ideas for life

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ENW89811J4CF 12/xx - Infinion's BlueMoon™ Universal Platform

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Rev1.0	Initial version
Rev2.0	Due to better range with another ceramic antenna, we have updated module height from 1.8mm to 2.8mm. Changes made in **"Production Package" on Page 28** If you need smaller height, let us discuss your individual case.
Rev3.0	Releasing this document and correct the ordering code to ENW89811J4CF

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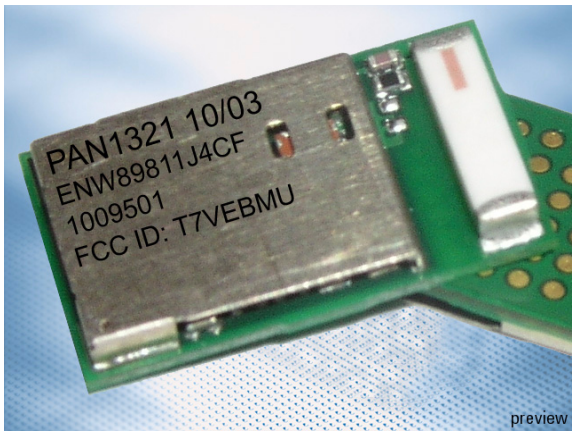
1 General Device Overview



1.1 Features

General

- Complete Bluetooth 2.0 + EDR solution
  - Configurable for BT 1.2
- Ultra low power design in 0.13 µm CMOS
- Temperature range from -40°C to 85°C
- Integrates ARM7TDMI, RAM and patchable ROM
- On-module voltage regulators. External supply 2.9 - 4.1 V
- On-module EEPROM with configuration data
- Reference clock included
- Low power clock from internal oscillator or external low power clock (e.g. 32.768 kHz)
- Dynamic low power mode switching

Interfaces

- AT command interface over UART, configurable from 9600 baud up to 3.25 MBaud
- General purpose I/Os with interrupt capabilities. JTAG for boundary scan and debug

RF

- Transmit power typ. 2.5 dBm (default settings)
- Receiver sensitivity typ. -86 dBm
- Integrated antenna switch, balun and antenna filter
- Integrated LNA with excellent blocking and intermodulation performance
- No external components except antenna
- Digital demodulation for optimum sensitivity and co-/adjacent channel performance

Bluetooth

- Bluetooth V2.0 + EDR compliant
- SPP Device A and B support 1 ACL link with stream or command mode
- SPP Device A and B - Visible while connected
- SPP Device A and B - Visible/connectable when not connected
- SPP Device A and B - Device Discovery capable after receiving OK on data transfer
- Sniff mode is supported with above capabilities
- 5 trusted devices stored in EEPROM
- Testing
- Enable DUT
- Crystal calibration
- H4 with UART HW flow control (RTS/CTS)
- Security modes: Modes 1 and Mode 3
- Master-Slave role switch

1.2 Block Diagram

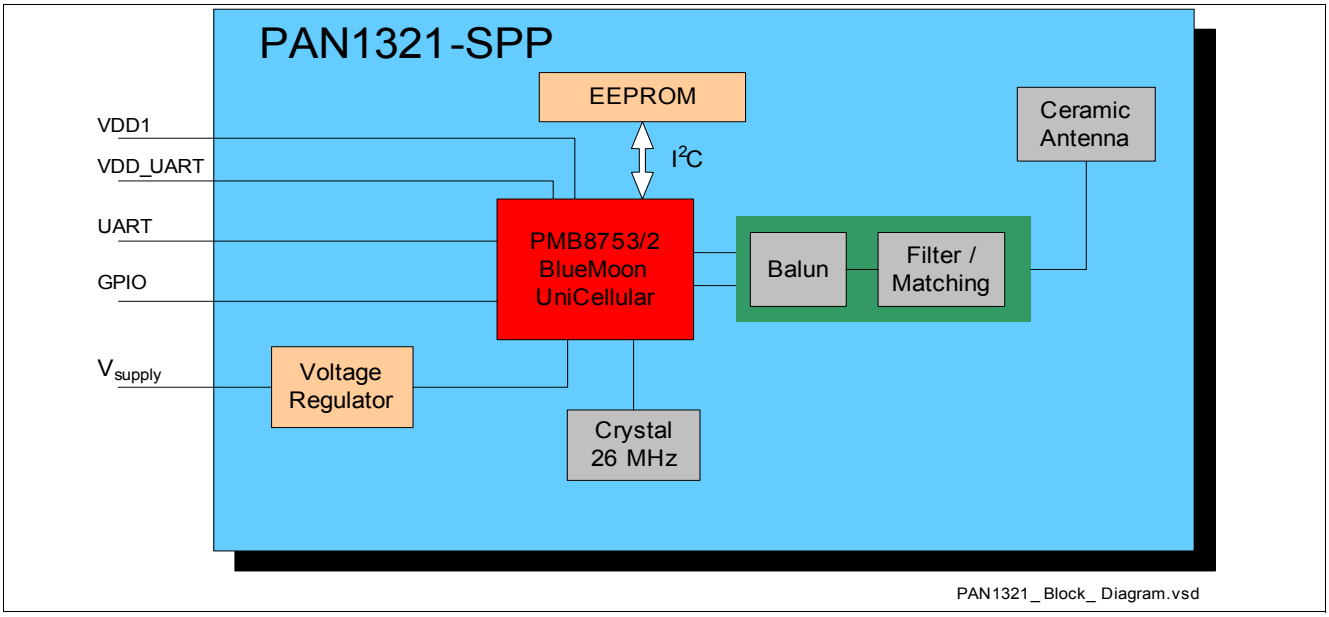


Figure 1 Simplified Block Diagram of PAN1321-SPP

1.3 Pin Configuration LGA

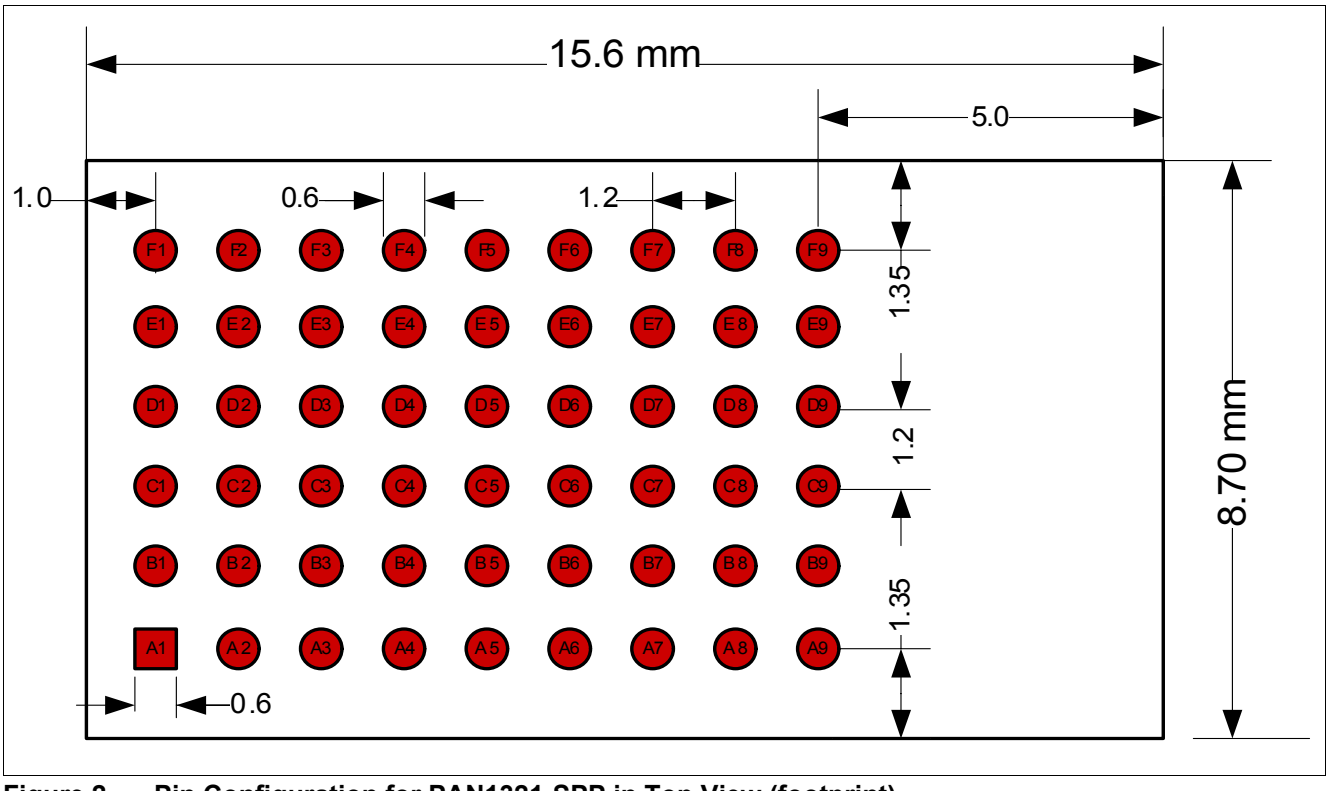


Figure 2 Pin Configuration for PAN1321-SPP in Top View (footprint)

1.4 Pin Description

The non-shaded cells indicate pins that will be fixed for the product lifetime. Shaded cells indicate that the pin might be removed/changed in future variants. Pins not listed below shall not be connected.

Table 1 Pin Description

Pin No.	Symbol	Input / Output	Supply Voltage	During Reset	After Reset	Function
A2	P1.6	I/O/OD	Internal1	Z	Z	Port 1.6
A3	RESET#	AI	Internal1	Input	Input	Hardware Reset
A8	P1.5	I/O/OD	Internal1	Input	Input	Port 1.5
B1	P1.7	I/O/OD	Internal1	PD/ Input	PD/ Input	Port 1.7
B2	P1.8	I/O/OD	Internal1	PD	PD	Port 1.8
B3	P1.0 / TMS	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.0 or JTAG interface
B4	P1.4 / RTCK	I/O/OD	Internal2	Z	Z	Port 1.4 or JTAG interface
B5	ONOFF	I		-	-	Turns off module completely
B9	SLEEPX	I/O	VDDUART	PD	H	Sleep indication signal
C2	P0.9	I/O/OD	Internal2	Z	Z	Port 0.9
C3	JTAG#	I	Internal2	PU	PU	Mode selection Port 1: 0: JTAG 1: Port
C4	TRST#	I	Internal2	PD	PD	JTAG interface
D1	P0.10	I/O/OD	Internal2	Z	Z	Port 0.10
D2	P0.8	I/O/OD	Internal2	PD	PD	Port 0.8
D3	P1.1 / TCK	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.1 or JTAG interface
D4	P0.3	I/O/OD	VDD1	Conf. PD def.	Conf. PD def.	Port 0.3
D5	P0.2	I/O/OD	VDD1	Z	Z	Port 0.2
E1	P0.12 / SDA0	I/O/OD	Internal2	PU	PU	I2C data signal
E2	P0.13 / SCL0	I/O/OD	Internal2	PU	PU	I2C clock signal
E3	P1.3 / TDO	I/O/OD	Internal2	Z	Z	Port 1.3 or JTAG interface
E4	P0.0	I/O/OD	VDD1	PD	PD	Port 0.0 LPM wakeup output
E5	P0.1	I/O/OD	VDD1	PD	PD	Port 0.1
E6	P0.5 / UARTRXD	I/O/OD	VDDUART	Z	Z	Port 0.5 or UART receive data
F2	P1.2 / TDI	I/O/OD	Internal2	PU[1)]	PU[1)]	Port 1.2 or JTAG interface
F3	P0.11	I/O/OD	Internal2	Z	Z	Port 0.11

Table 1 Pin Description

Pin No.	Symbol	Input / Output	Supply Voltage	During Reset	After Reset	Function
F4	P0.14	I/O	VDDUART	Z	Z	Port 0.14 LPM wakup input
F5	P0.7 / UARTCTS	I/O/OD	VDDUART	Z	Z	Port 0.7 or UART CTS flow control
F7	P0.4 / UARTTXD	I/O/OD	VDDUART	PU	PU	Port 0.4 or UART transmit data
F8	P0.6 / UARTRTS	I/O/OD	VDDUART	PU	PU	Port 0.6 or UART RTS flow control
A4, A5, A6	VSUPPLY	SI		-	-	Power supply
C1	VREG	SO		-	-	Regulated Power supply
F6	VDDUART	SI		-	-	UART interface Power supply
C5	VDD1	SI		-	-	Power supply
A1, A7, A9, C8, C9, D7, D8, E8, E9, F1, F9	VSS			-	-	Ground

1) Fixed pull-up/pull-down if JTAG interface is selected, not affected by any chip reset. If JTAG interface is not selected the port is tristate.

Descriptions of acronyms used in the pin list:

Acronym	Description
I	Input
O	Output
OD	Output with open drain capability
Z	Tristate
PU	Pull-up
PD	Pull-down
A	Analog (e.g. AI means analog input)
S	Supply (e.g. SO means supply output)

1.5 System Integration

PAN1321-SPP is optimized for a low bill of material (BOM) and a small PCB size. **Figure 3** shows a typical application example.

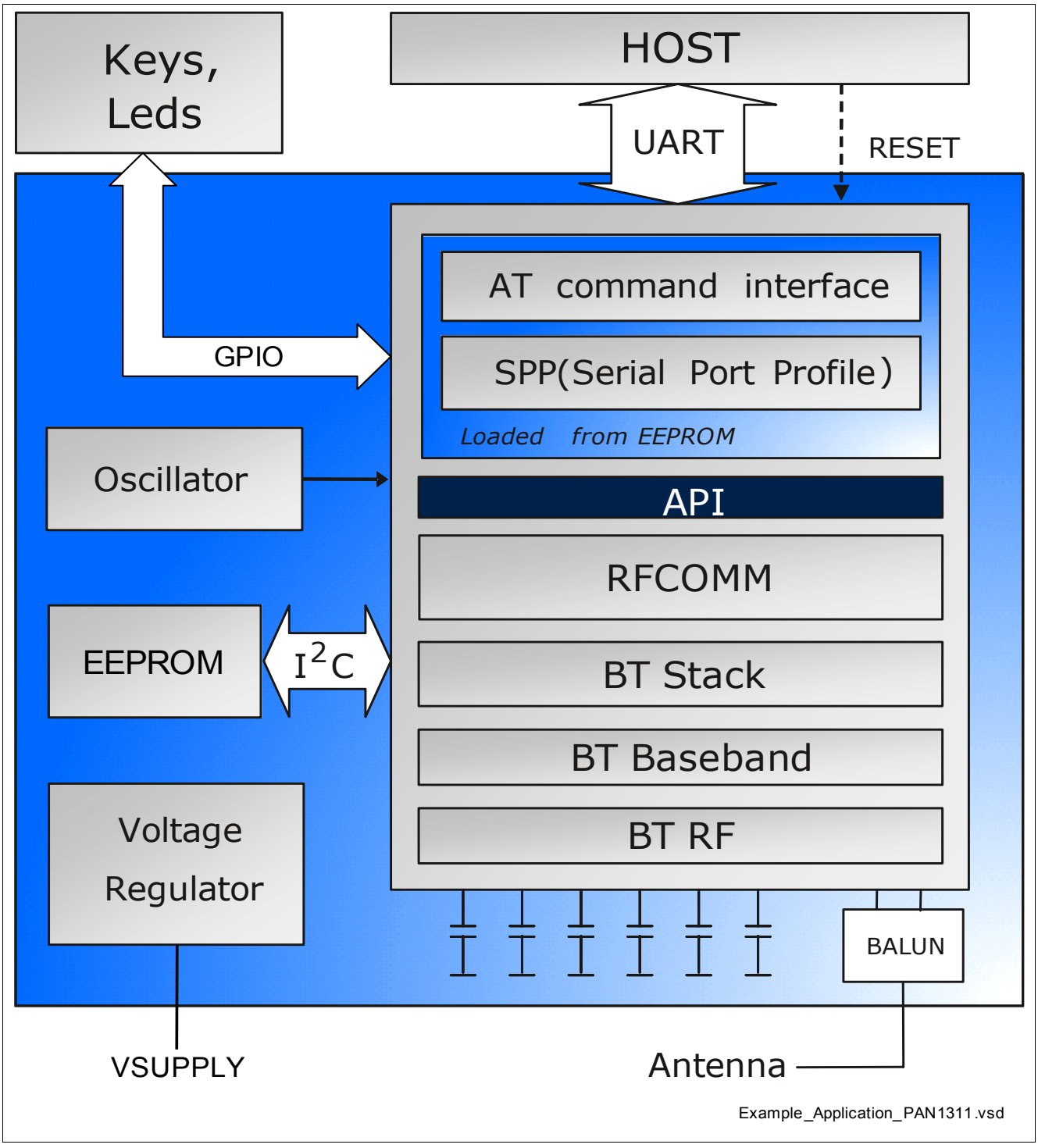


Figure 3 Example of a Bluetooth System using eUniStone

The UART interface is used for communication between the host and PAN1321-SPP. The lines UARTTXD and UARTRXD are used for commands, events and data. The lines UARTRTS and UARTCTS are used for hardware flow control.

Low power mode control of PAN1321-SPP and the host can be implemented in by using the pins P0.14 and P0.0. P0.14 is used by the host to allow PAN1321-SPP to enter low power mode and P0.0 is used by PAN1321-SPP to wake-up the host when attention is required. Additionally, the host could hardware reset PAN1321-SPP using the RESET# pin.

Power is supplied to a single VSUPPLY input from which internal regulators can generate all required voltages. The UART and the GPIO's interfaces have separate supply voltages so that they can comply with host signaling.

1.6 FW version

PAN1321-SPP is available in different versions. Please check corresponding release documents for latest information. The identifier about the software version will be visible on the module, please refer to **Figure 5**, here it is xx.

2 Basic Operating Information

2.1 Power Supply

PAN1321-SPP is supplied from a single supply voltage VSUPPLY. This supply voltage must always be present. The PAN1321-SPP chip is supplied from an internally generated 2.5 V supply voltage. This voltage can be accessed from the VREG pin. This voltage may not be used for supplying other components in the host system but can be used for referencing the host interfaces.

The GPIO's and the UART interface are supplied with dedicated, independent, reference levels via the VDD1 and VDDUART pins. All other digital I/O pins are supplied internally by either 2.5 V (Internal2) or 1.5 V (Internal1). **Section 1.4** provides a mapping between pins and supply voltages.

The I/O power domains (VDD1 and VDDUART) are completely separated from the other power domains and can stay present also in low power modes.

2.2 Clocking

PAN1321-SPP contains a crystal from which the internal 26 MHz system clock is generated. Also, the low power mode clock of 32 kHz is generated internally, which means that no external clock is needed.

3 Interfaces

3.1 UART Interface

The UART interface is the main communication interface between the host and PAN1321-SPP.

The interface consists of four UART signals and two wake-up signals as shown in **Figure 4**.

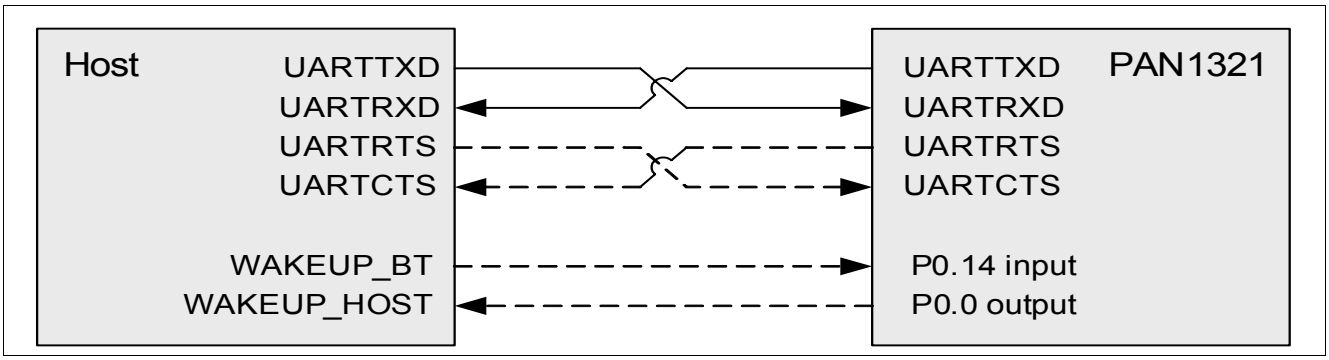


Figure 4 UART Interface

3.1.1 UART

The UART (Universal Asynchronous Receiver and Transmitter) interface is compatible with standard UART H4 (4-wire). The lines UARTTXD and UARTRXD are used for commands, events and data. The lines UARTRTS and UARTCTS are used for hardware flow control. A separate supply voltage, VDDUART, makes it easy to connect the UART interface to any system.

3.1.1.1 Baud Rates

The supported baud rates are listed in **Table 2** together with the small deviation error that results from the internal clock generation. The default baud rate is 115200 Baud.

Table 2 UART Baud Rates

Wanted Baud Rate	Real Baud Rate	Deviation Error (%)
9600	9615	0.16
19200	19230	0.16
38400	38461	0.16
57600	57522	-0.14
115200	115044	-0.14
230400	230088	-0.14
460800	464285	0.76
921600	928571	0.76
1843200	1857142	0.76
3250000	3250000	0

4 General Device Capabilities

This chapter describes features available in the PAN1321 (ENW89811J4CF 12/xx) core.

Actual feature set and how to access the features can be found in the AT Command document [1]. Release specific performance characteristics, like data speed, is related in the SW Release Notes [2].

4.1 HCI+

The PAN1321 module can be programmed over UART with a specific application for RF test purposes, like TX continuous or TX burst mode. This test application is controlled over the UART through Infineon specific HCI commands. The commands supported by this test application are described in the document “T8753-2-Infineon_Specific_HCI_Commands-7600.pdf”.

4.2 Firmware ROM Patching

4.2.1 Patch Support

PAN1321-SPP contains dedicated hardware that makes it possible to apply patches to the code and data in the firmware ROM. The hardware is capable of replacing up to 32 blocks of 16 bytes each with new content. This area can be filled with any combination of code and data. The firmware patch is stored in EEPROM and automatically loaded after startup. This provides a flexible bugfix solution for the ROM part of the firmware.

5 Bluetooth Capabilities

5.1 Supported Features

- Bluetooth V2.0 + EDR compliant
- Enhanced Data Rate up to 3 Mbit/s
- Adaptive Frequency Hopping (AFH)
- All packet types
- Authentication, Pairing and Encryption
- SPP Device A and B support 1 ACL link with stream or command mode
- SPP Device A and B - Visible while connected
- SPP Device A and B - Visible/connectable when not connected
- SPP Device A and B - Device Discovery capable after receiving OK on data transfer
- Sniff mode is supported with above capabilities
- 5 trusted devices stored in EEPROM
- Enable DUT
- Crystal calibration
- H4 with UART HW flow control (RTS/CTS)
- Security modes: Modes 1 and Mode 3
- Master-Slave role switch
- Quality of Service
- Channel Quality Driven Data Rate change
- Sniff, Hold
- Role Switch
- RSSI and Power Control
- Power class 2 and 3
- Standard Bluetooth test mode, Active Tester Mode and RF Test Modes

5.2 PAN1321-SPP Specifics and Extensions

5.2.1 During Connection

5.2.1.1 Role Switch

Only one role switch can be performed at a time. If a role switch request is pending, other role switch requests on the same or other links are rejected. If a role switch fails, PAN1321-SPP will automatically try again a maximum of three times. Encryption (if present) is stopped in the old piconet before a role switch is performed and re-enabled when the role switch has succeeded or failed.

5.2.1.2 Dynamic Polling Strategy

In addition to the regular polling scheme, PAN1321-SPP dynamically assigns unused slots to links where data is exchanged. This adapts very well to bursty traffic and improves throughput and latency on the links.

5.2.1.3 Adaptive Frequency Hopping (AFH)

PAN1321-SPP supports adaptive frequency hopping according to the Bluetooth 2.0 + EDR specification. AFH switch and channel classification are supported both as master and slave. Channel classification from the host is also supported.

A number of HCI+ commands and events are available to provide information about AFH operation. The commands Infineon_Enable_AFH_Info_Sending and Infineon_Disable_AFH_Info_Sending turn on and off the Infineon AFH Info events that provide detailed information about channel classification, channel maps, interferers, etc.

If enabled by the Infineon_Enable_Infineon_Events command, the Infineon AFH Extraordinary RSSI event informs the host whenever extraordinary RSSI measurements in unused slots have been started. This is done when the number of known good channels has decreased below a critical limit and periodically after a defined time.

The Infineon_Set_AFH_Measurement_Period command can be used to configure the duration of the AFH measurement period.

5.2.1.4 Channel Quality Driven Data Rate Change (CQDDR)

PAN1321-SPP supports channel quality driven data rate change according to the Bluetooth 2.0 + EDR specification. A device that receives an LMP_preferred_rate message is not required to follow all recommendations. PAN1321-SPP normally at least follows the recommendation whether to use forward error correction (FEC) or not. If possible, recommendations about packet size and modulation scheme will be taken into account. When PAN1321-SPP sends an LMP_preferred_rate to another device the proposal always includes preferences for all parameters.

The HCI+ commands Infineon_Enable_CQDDR_Info_Sending and Infineon_Disable_CQDDR_Info_Sending turn on and off sending of the Infineon CQDDR Info event. This event provides information to the host every time a new CQDDR proposal is sent to a remote device.

5.2.2 RSSI and Output Power Control

5.2.2.1 Received Signal Strength Indication (RSSI)

PAN1321-SPP supports received signal strength measurements and uses LMP signaling to keep the output power of a remote device within the golden receive power range. The range is set with the BD_DATA parameters RSSI_Min and RSSI_Max.

5.2.2.2 Output Power Control

PAN1321-SPP supports power control according to the Bluetooth 2.0+EDR specification.

- The output power can be controlled in up to 4 configurable steps. PAN1321-SPP can work as a class 2 or 3 device, depending on the settings.
- Fine tuning can be used on the power steps.
- A default sub-state power step can be set

The power step configuration is set through BD_DATA parameters.

The Inquiry output power can be programmed with the Write Inquiry Transmit Power Level command introduced in the 2.0 Bluetooth Core specification.

5.2.2.3 Ultra Low Transmit Power

For high security devices the output power can be reduced to a value that reduces the communication range to a few inches. This mode is enabled with the HCI+ command Infineon_TX_Power_Config.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature		-40	–	125	°C	–
VSUPPLY supply voltage		-0.3	–	6.0	V	–
VDDUART supply voltage		-0.9	–	4.0	V	–
VDD1 supply voltage		-0.9	–	4.0	V	–
VREG		-0.3	–	4.0	V	VSUPPLY > 4 V
VREG		-0.3	–	VSUPPLY	V	VSUPPLY < 4 V
ONOFF		-0.3	–	VSUPPLY+0.3	V	
Input voltage range		-0.9	–	4.0	V	–
Output voltage range		-0.9	–	4.0	V	-9
ESD		–	–	1.0	kV	According to MIL-STD883D method 3015.7

Note: Stresses above those listed here are likely to cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.
Maximum ratings are not operating conditions.

6.2 Operating Conditions

Table 4 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operating temperature		-40	–	85[1)]	°C	–
Main supply voltage (Vsupply)		2.9	–	4.1	V	–
VDDUART		1.35	–	3.6	V	–
VDD1		1.35	–	3.6	V	–

1) For Version 10/0x: only 70°C

6.3 DC Characteristics

6.3.1 Pad Driver and Input Stages

For more information, see **Chapter 1.4**.

Table 5 Internal1 (1.5 V) Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.27	V	–
Input high voltage		1.15	–	3.6	V	–
Output low voltage		–	–	0.25	V	IOL = 1 mA
Output high voltage		1.1	–	–	V	IOH = -1 mA
Continuous Load[1)]		–	–	1	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all Internal1 supplied pins shall not exceed 2mA at the same time

Table 6 Internal2 (2.5 V) Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.45	V	–
Input high voltage		1.93	–	2.8	V	P0.10
Input high voltage		1.93	–	3.6	V	Other pins
Output low voltage		–	–	0.25	V	IOL = 5 mA
Output low voltage		–	–	0.15	V	IOL = 2 mA
Output high voltage		2.0	–	–	V	IOH = -5 mA
Output high voltage		2.1	–	–	V	IOH = -2 mA
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all Internal2 supplied pins shall not exceed 35 mA at the same time

Table 7 VDDUART Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.2*VDDUART	V	–
Input high voltage		0.7*VDDUART	–	VDDUART+0.3	V	P0.5/UARTRXD
Input high voltage		0.7*VDDUART	–	3.6	V	Other pins

Table 7 VDDUART Supplied Pins (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output low voltage		–	–	0.25	V	IOL = 5 mA VDDUART = 2.5 V
Output low voltage		–	–	0.15	V	IOL = 2 mA VDDUART = 2.5 V
Output high voltage		VDDUART -0.25	–	–	V	IOH = -5 mA VDDUART = 2.5 V
Output high voltage		VDDUART -0.15	–	–	V	IOH = -2 mA VDDUART = 2.5 V
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all VDDUART supplied pins shall not exceed 35 mA at the same time

Table 8 VDD1 Supplied Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		-0.3	–	0.2*VDD1	V	–
Input high voltage		0.7*VDD1	–	3.6	V	–
Output low voltage		–	–	0.25	V	IOL = 5 mA VDD1 = 2.5 V
Output low voltage		–	–	0.15	V	IOL = 2 mA VDD1 = 2.5 V
Output high voltage		VDD1 -0.25	–	–	V	IOH = -5 mA VDD1 = 2.5 V
Output high voltage		VDD1 -0.15	–	–	V	IOH = -2 mA VDD1 = 2.5 V
Continuous Load[1)]		–	–	5	mA	–
Pin Capacitance		–	–	10	pF	–
Magnitude Pin Leakage		–	0.01	1	µA	Input and output drivers disabled

1) The totaled continuous load for all VDD1 supplied pins shall not exceed 35 mA at the same time

Table 9 ONOFF PIN

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage		–	–	0.7	V	–
Input high voltage		1.7	–	VSUPPLY	V	–
Input current		-1	0.01	1	µA	ONOFF = 0 V

6.3.2 Pull-ups and Pull-downs

Table 10 Pull-up and Pull-down Currents

Pin	Pull Up Current			Pull Down Current			Unit	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
P0.12 P0.13	260	740	1300	N/A	N/A	N/A	µA	Pull-up current measured with pin voltage = 0 V Pull-down current measured with pin voltage = supply voltage Min measured at 125°C with supply = 1.35 V Typ. measured at 27°C with supply = 2.5V Max measured at -40°C with supply = 3.63 V
P0.0 P0.1 P0.2 P0.3	22	130	350	23	150	380	µA	
P0.4 P0.5 P0.6 P0.7 P0.10 P0.8 P0.9 P0.11 P0.14 P0.15	4.2	24	68	3.0	20	55	µA	
P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7 P1.8	1.1	6.0	17	0.75	5.0	14	µA	

6.3.3 Protection Circuits

All pins have an inverse protection diode against VSS.
P0.10 has an inverse diode against Internal2.
P0.5/UARTRXD has an inverse diode against VDDUART.
All other pins have no diode against their supply.

6.3.4 System Power Consumption

Table 11 Max. Load at the Different Supply Voltages

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Vsupply		–	–	100	mA	Peak current

Note: I/O currents are not included since they depend mainly on external loads.

6.4 AC Characteristics

6.5 RF Part

6.5.1 Characteristics RF Part

The characteristics involve the spread of values to be within the specific temperature range. Typical characteristics are the median of the production.

All values refers to Infineon reference design. All values will be updated after verification/Characterisation.

6.5.1.1 Bluetooth Related Specifications

Table 12 BDR - Transmitter Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output power (high gain)		0.5	2.5	4.5	dBm	Default settings
Output power (highest gain)		–	4.5	–	dBm	Maximum settings
Power control step size		4	6	8	dB	–
Frequency range fL		2400	2401.3	–	MHz	–
Frequency range fH		–	2480.7	2483.5	MHz	–
20 dB bandwidth		–	0.930	1	MHz	–
2nd adjacent channel power		–	-40	-20	dBm	–
3rd adjacent channel power		–	-60	-40	dBm	–
>3rd adjacent channel power		–	-64	-40	dBm	Max. 2 of 3 exceptions @ 52 MHz offset might be used
Average modulation deviation for 00001111 sequence		140	156	175	kHz	–
Minimum modulation deviation for 01010101 sequence		115	145	–	kHz	–
Ratio Deviation 01010101 / Deviation 00001111		0.8	1	–		–
Initial carrier frequency tolerance |foffset|		–	–	75	kHz	–

Table 12 BDR - Transmitter Part (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Carrier frequency drift (one slot) |fdrift|		–	10	25	kHz	–
Carrier frequency drift (three slots) |fdrift|		–	10	40	kHz	–
Carrier frequency drift (five slots) |fdrift|		–	10	40	kHz	–
Carrier frequency driftrate (one slot) |fdriftrate|		–	5	20	kHz/50 ms	–
Carrier frequency driftrate (three slots) |fdriftrate|		–	5	20	kHz/50 ms	–
Carrier frequency driftrate (five slots) |fdriftrate|		–	5	20	kHz/50 ms	–

Table 13 BDR -Receiver Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sensitivity		–	-86	-81	dBm	Ideal wanted signal
C/I-performance: -4th adjacent channel		–	-51	-40	dB	–
C/I-performance: -3rd adjacent channel (1st adj. of image)		–	-46	-20	dB	–
C/I-performance: -2nd adjacent channel (image)		–	-35	-9	dB	–
C/I-performance: -1st adjacent channel		–	-4	0	dB	–
C/I-performance: co. channel		–	9	11	dB	–
C/I-performance: +1st adjacent channel		–	-4	0	dB	–
C/I-performance: +2nd adjacent channel		–	-40	-30	dB	–
C/I-performance: +3rd adjacent channel		–	-50	-40	dB	–
Blocking performance 30 MHz - 2 GHz		10	–	–	dBm	Some spurious responses, but according to BT-specification
Blocking performance 2 GHz - 2.4 GHz		-27	–	–	dBm	–
Blocking performance 2.5 GHz - 3 GHz		-27	–	–	dBm	–
Blocking performance 3 GHz - 12.75 GHz		10	–	–	dBm	Some spurious responses, but according to BT-specification

Table 13 BDR -Receiver Part (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Intermodulation performance		-39	-34	–	dBm	Valid for all intermodulation tests
Maximum input level		-20	–	–	dBm	–

Table 14 EDR - Transmitter Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output power (high gain)		-2.5	–	2	dBm	
Relative transmit power: PxPSK - PGFSK		-4	-0.6	1	dB	
Carrier frequency stability |ωi|		–	–	75	kHz	–
Carrier frequency stability |ωi+ω0|		–	–	75	kHz	–
Carrier frequency stability |ω0|		–	2	10	kHz	–
DPSK - RMS DEVM		–	10	20	%	–
8DPSK - RMS DEVM		–	10	13	%	–
DPSK - Peak DEVM		–	20	35	%	–
8DPSK - Peak DEVM		–	20	25	%	–
DPSK - 99% DEVM		–	–	30	%	–
8DPSK - 99% DEVM		–	–	20	%	–
Differential phase encoding		99	100	–	%	–
1st adjacent channel power		–	-40	-26	dBc	–
2nd adjacent channel power		–	–	-20	dBm	Carrier power measured at basic rate
3rd adjacent channel power		–	–	-40	dBm	Carrier power measured at basic rate

Table 15 EDR -Receiver Part

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DQPSK-Sensitivity		–	-88	-83	dBm	Ideal wanted signal
8DPSK-Sensitivityl		–	-83	-77	dBm	Ideal wanted signal
DQPSK - BER Floor Sensitivity		–	-84	-60	dBm	–
8DPSK - BER Floor Sensitivity		–	-79	-60	dBm	–
DQPSK - C/I-performance: -4th adjacent channel		–	-53	-40	dB	–
DQPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		–	-47	-20	dB	–
DQPSK - C/I-performance: -2nd adjacent channel (image)		–	-31	-7	dB	–

Table 15 EDR -Receiver Part (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DQPSK - C/I-performance: -1st adjacent channel		–	-7	0	dB	–
DQPSK - C/I-performance: co. channel		–	11	13	dB	–
DQPSK - C/I-performance: +1st adjacent channel		–	-9	0	dB	–
DQPSK - C/I-performance: +2nd adjacent channel		–	-44	-30	dB	–
DQPSK - C/I-performance: +3rd adjacent channel		–	-50	-40	dB	–
8DPSK - C/I-performance: -4th adjacent channel		–	-48	-33	dB	–
8DPSK - C/I-performance: -3rd adjacent channel (1st adj. of image)		–	-44	-13	dB	–
8DPSK - C/I-performance: -2nd adjacent channel (image)		–	-25	0	dB	–
8DPSK - C/I-performance: -1st adjacent channel		–	-5	5	dB	–
8DPSK - C/I-performance: co. channel		–	17	21	dB	–
8DPSK - C/I-performance: +1st adjacent channel		–	-5	5	dB	–
8DPSK - C/I-performance: +2nd adjacent channel		–	-36	-25	dB	–
8DPSK - C/I-performance: +3rd adjacent channel		–	-46	-33	dB	–
Maximum input level		-20	–	–	dBm	–

7 Package Information

7.1 Package Marking

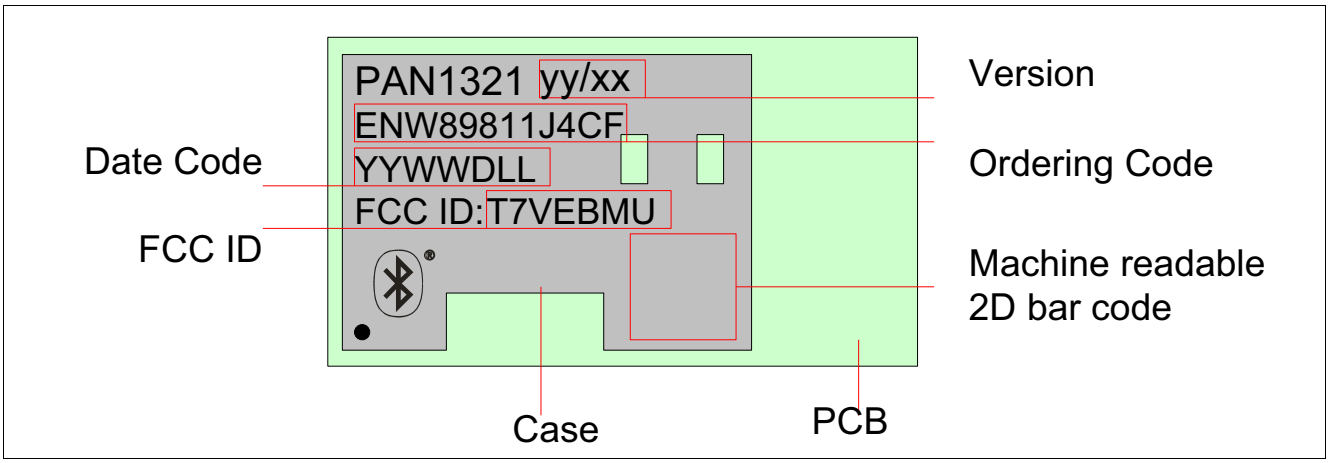


Figure 5 Package Marking

7.2 Production Package

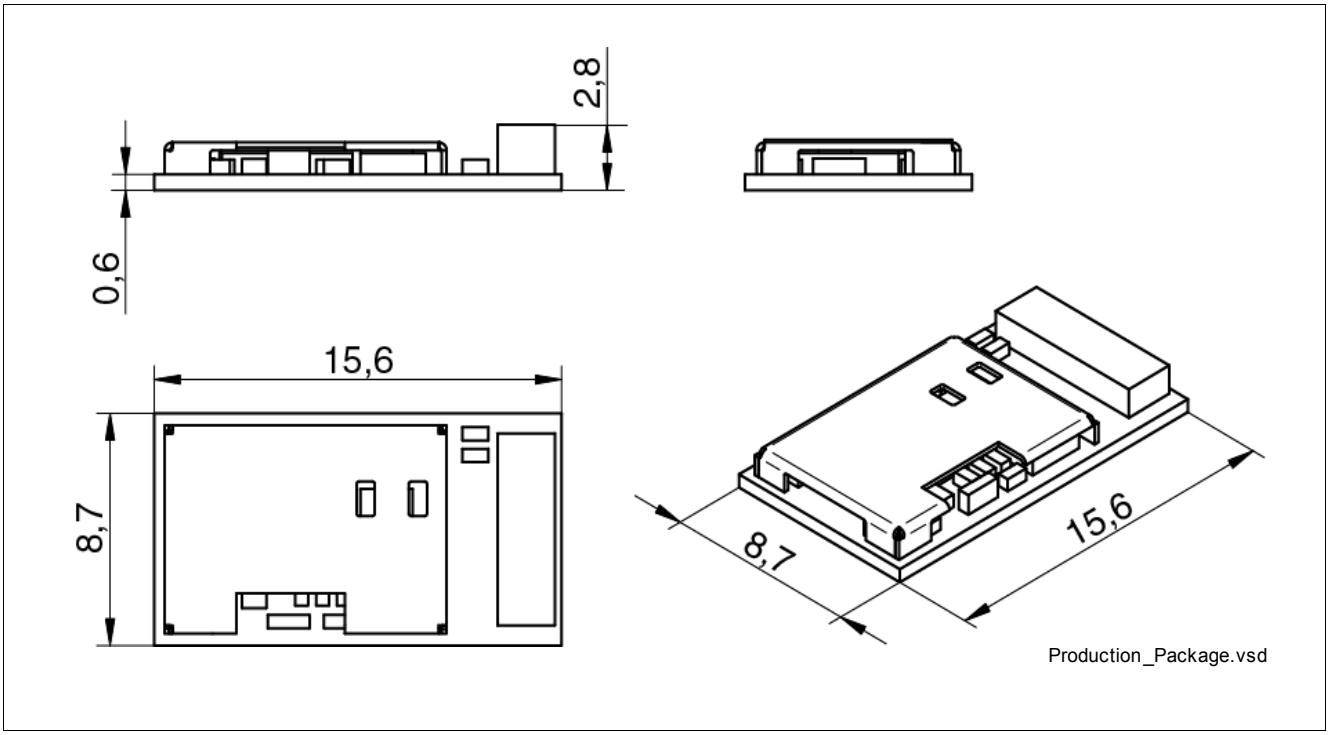


Figure 6 Production Package

All dimensions are in mm.

Tolerances on all outer dimensions, height, width and length, are +/- 0.2 mm.

7.2.1 Pin Mark

Pin 1 (A1) is marked on bottom footprint and on the top of the shield on the module according to **Figure 7**. Diameter of pin 1 mark on the shield is 0.15 mm.

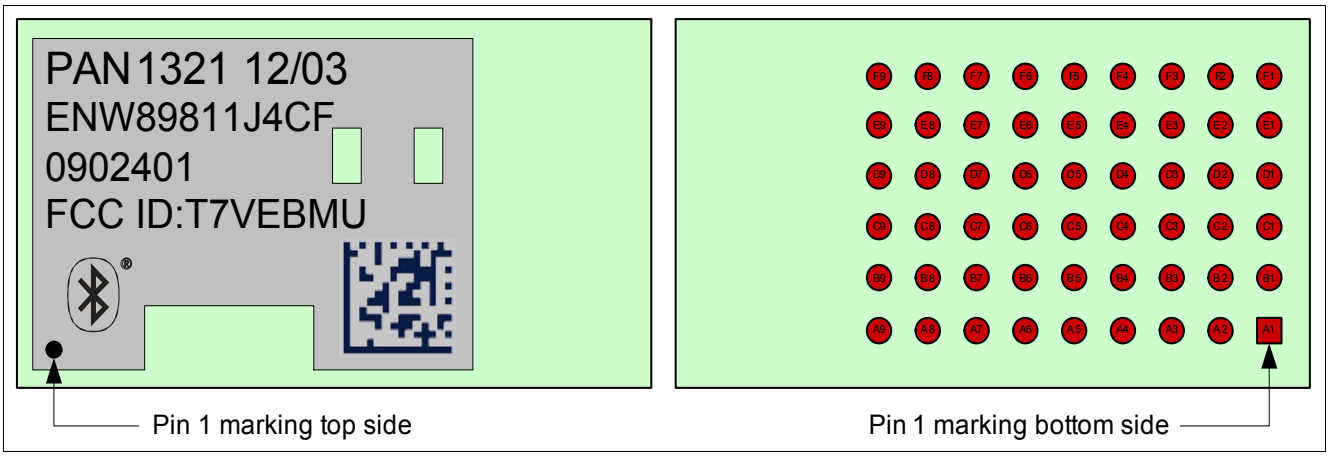


Figure 7 Top View and Bottom View

8 Assembly Guidelines

The target of this document is to provide guidelines for customers to successfully introduce the PAN1321-SPP module in production. This includes general description, PCB-design, solder printing process, assembly, soldering process, rework and inspection.

8.1 General Description of the Module

PAN1321-SPP is a Land Grid Array (LGA 6x9) module made for surface mounting. The pad diameter is 0.6 mm and the pitch 1.2 mm.

All solder joints on the module will reflow during soldering on the mother board. All components and shield will stay in place due to wetting force. Wave soldering is not possible.

Surface treatment on the module pads is Nickel (5 - 8 µm)/Gold (0.04 - 0.10 µm).

Figure 8 shows the pad layout on the module, seen from the component side.

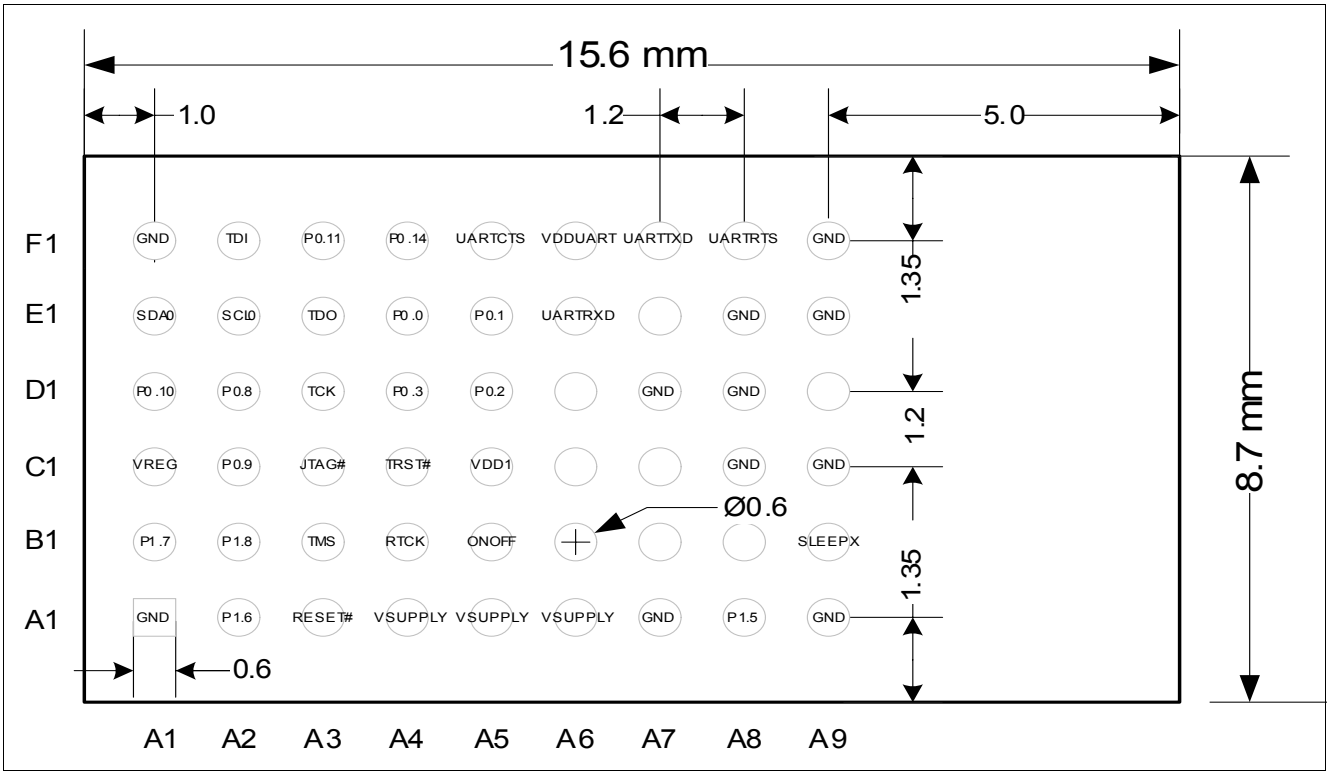


Figure 8 Pad Layout on the Module (top view)

8.2 Printed Circuit Board Design

The land pattern on the PCB shall be according to the land pattern on the module, which means that the diameter of the LGA pads on the PCB shall be 0.6 mm. It is recommended that each pad on the PCB shall be surrounded by a solder mask clearance of about 75 µm to avoid overlapping solder mask and pad.

8.3 Solder Paste Printing

The solder paste deposited on the PCB by stencil printing has to be of eutectic or near eutectic tin leadfree / lead composition. A no-clean solder paste is preferred, since cleaning of the solder joints is difficult because of the small gap between the module and the PCB.

Preferred thickness of the solder paste stencil is 100 - 127 µm (4 - 5 mils). The apertures on the solder paste stencil shall be of the same size as the pads, 0.6 mm.

8.4 Assembly

8.4.1 Component Placement

In order to assure a high yield, good placement on the PCB is necessary. As a rule of thumb the tolerable misplacement is 150 µm. This means that the PAN1321 module can be assembled with a variety of placement systems.

It is recommended to use a vision system capable of package pad recognition and alignment that evaluates the pad locations on the package (in contrast to outline centring). This eliminates the pad to package edge tolerance.

The recommendation is to pick and place the module with a nozzle in the centre of the shield. The nozzle diameter shall not be bigger than 4 mm.

8.4.2 Pin Mark

Pin 1 (A1) is marked on bottom footprint and on the top of the shield on the module according to **Figure 9**. Diameter of pin 1 mark on the shield is 0.15 mm.

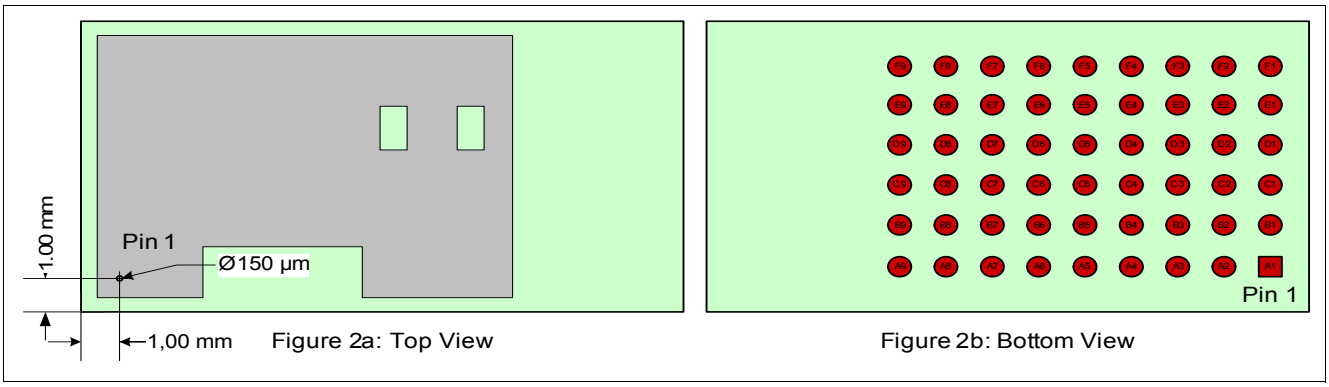


Figure 9 Pin Marking

8.4.3 Package

PAN1321 is packed in tape on reel according to **Figure 10**.

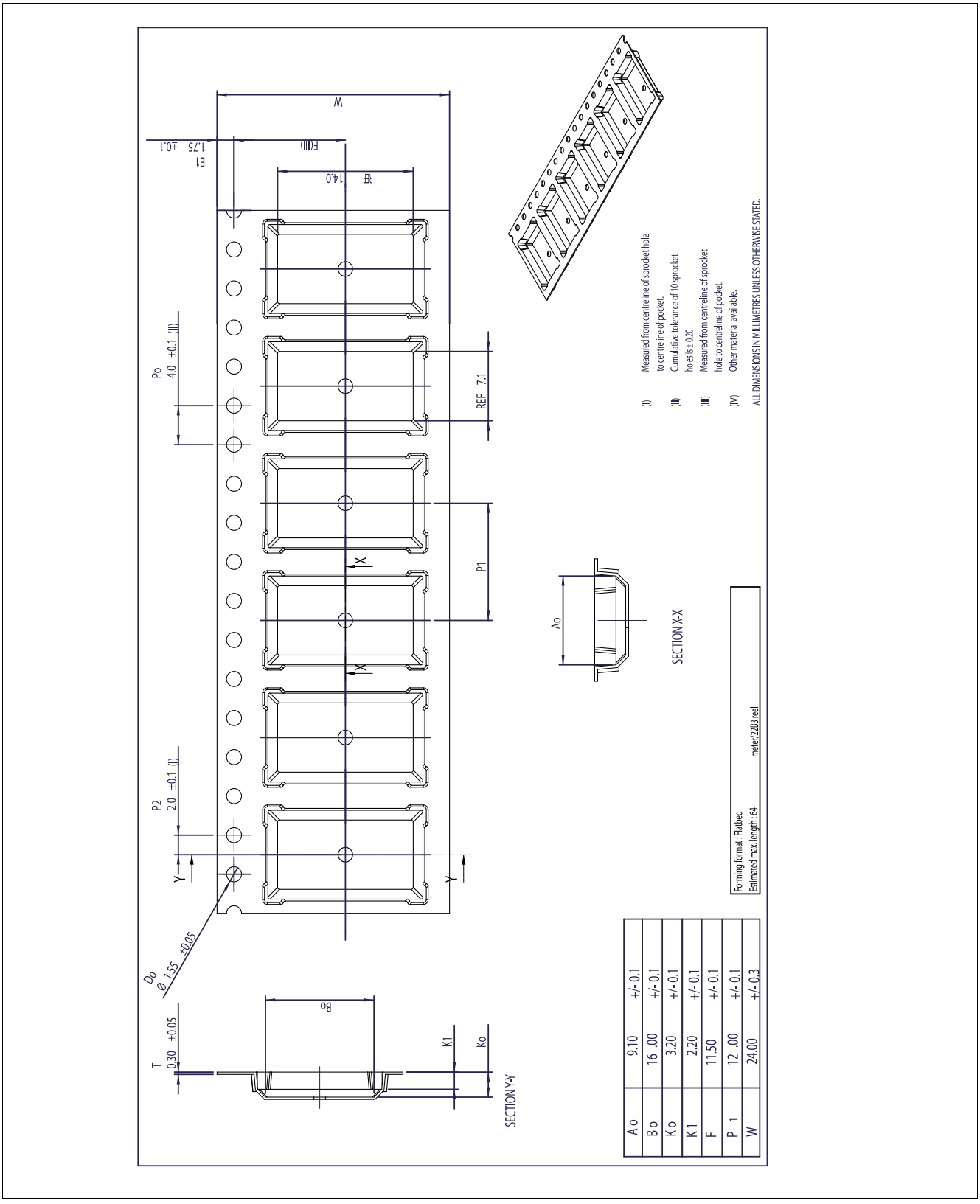


Figure 10 Tape on Reel

8.5 Soldering Profile

Generally all standard reflow soldering processes (vapour phase, convection, infrared) and typical temperature profiles used for surface mount devices are suitable for the PAN1321 module. **Wave soldering is not possible.**

Figure 11 and Figure 12 shows example of a suitable solder reflow profile. One for leaded and one for leadfree solder.

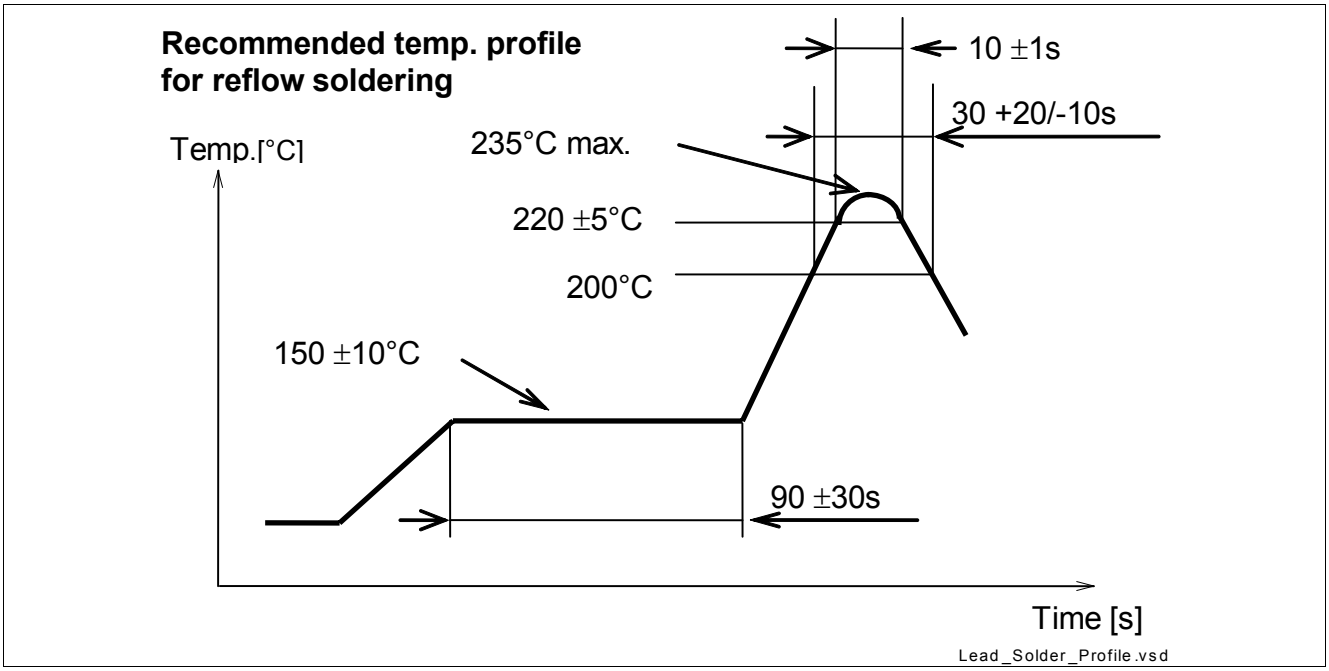


Figure 11 Eutectic Lead-Solder Profile

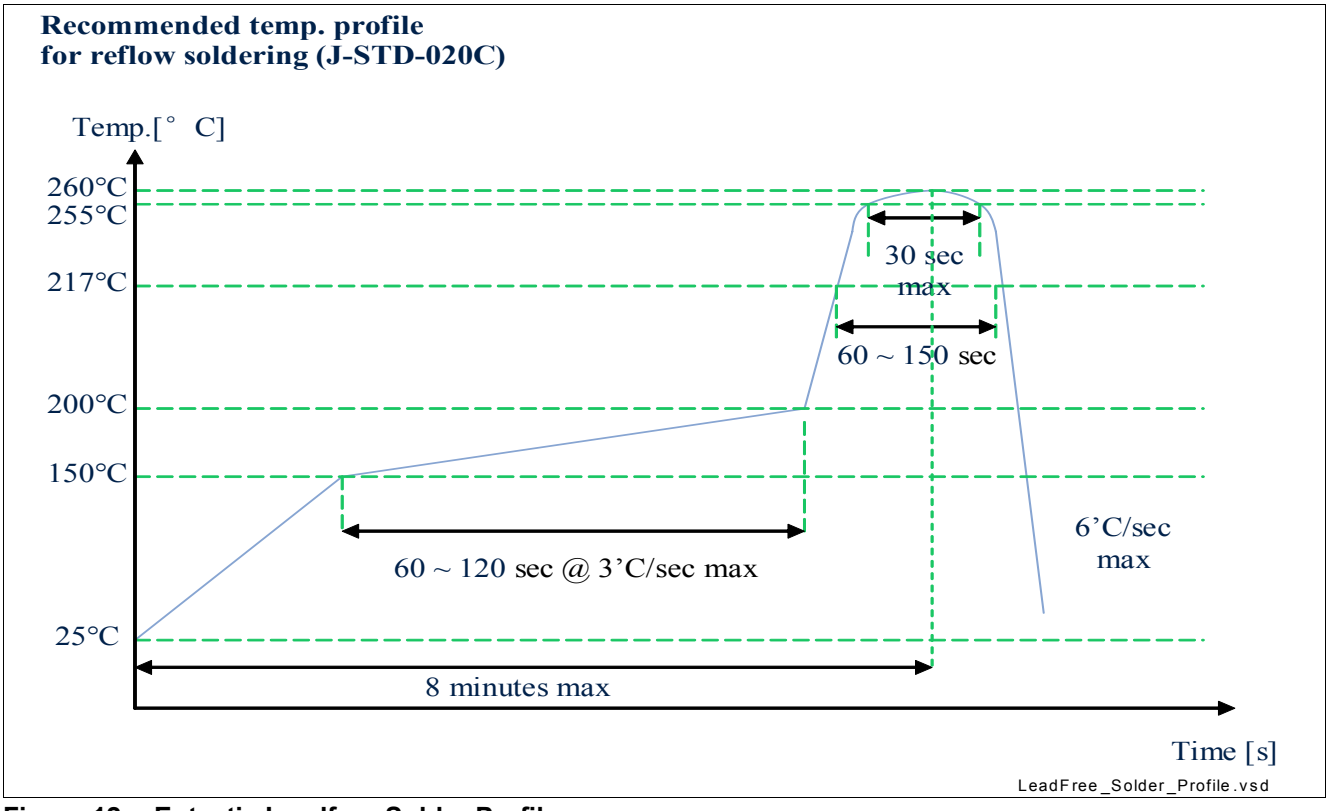


Figure 12 Eutectic Leadfree-Solder Profile

At the reflow process each solder joint has to be exposed to temperatures above solder liquids for a sufficient time to get the optimum solder joint quality, whereas overheating the board with its components has to be avoided. Using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB (especially on large, complex boards with different thermal masses of the components). The most recommended types are therefore forced convection or vapour phase reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary.

The reflow profiles and other reflow parameters are dependent on the used solder paste. The paste manufacturer provides a reflow profile recommendation for this product.

Additionally it is important not to overheat the PAN1321 module by a too large reflow peak temperature. PAN1321 contain several plastic packages and is there by sensitive of the moisture content level at the time of board assembly.

Overheating in combination with excessive moisture content could result in package delaminations or cracks (popcorn effect). The heating rate should not exceed 3°C/s and max sloping rate should not exceed 4°C/s.

PAN1321 shall be handled according to MSL3, which means a floor life of 168h in 30°C/60% r.h.

The PAN1321 module can be soldered according to max. J-STD-020C curve, assuming that all other conditions are followed stated in Product Specification, Qualification Report and in Application Note. Restriction is that PAN1321 can be soldered two times, since one time is already consumed when soldering devices on Module.

8.6 Rework

8.6.1 Removal Procedure

1. Heat the module with an appropriate heating nozzle according to the instruction of the equipment or on a hot plate (about 225°C dependent on the board). Hot plate can only be used if the board is single side assembled. The temperature of the module shall be 200-220°C.
2. Use grippers or a pair of tweezers to remove the module. The module has to be gripped on two opposite edges of the module (not on the shield).
3. Remove excess solder by using solder sucker, suction soldering irons or solder wick.

8.6.2 Replacement Procedure

Replacement can be done in two ways, dependent of how the solder is applied. Solder can be applied either by dispensing on the mother board or by printing the solder paste directly on the module.

8.6.2.1 Alternative 1: Dispensing Solder

A dispenser with controlled volume must be used to assure the same volume on every pad. The volume on each pad shall be about 0.04 mm^3.

1. Dispense 0.04 mm^3 on each LGA pad
2. Pick the module by a nozzle and place in the right position on the board
3. Reflow the solder.

8.6.2.2 Alternative 2: Printing Solder

To print solder on the module a fixture must be used. The purpose of the fixture is to get a flat surface and fix the stencil and module for printing. An example of how this fixture can be designed is shown in **Figure 13**.

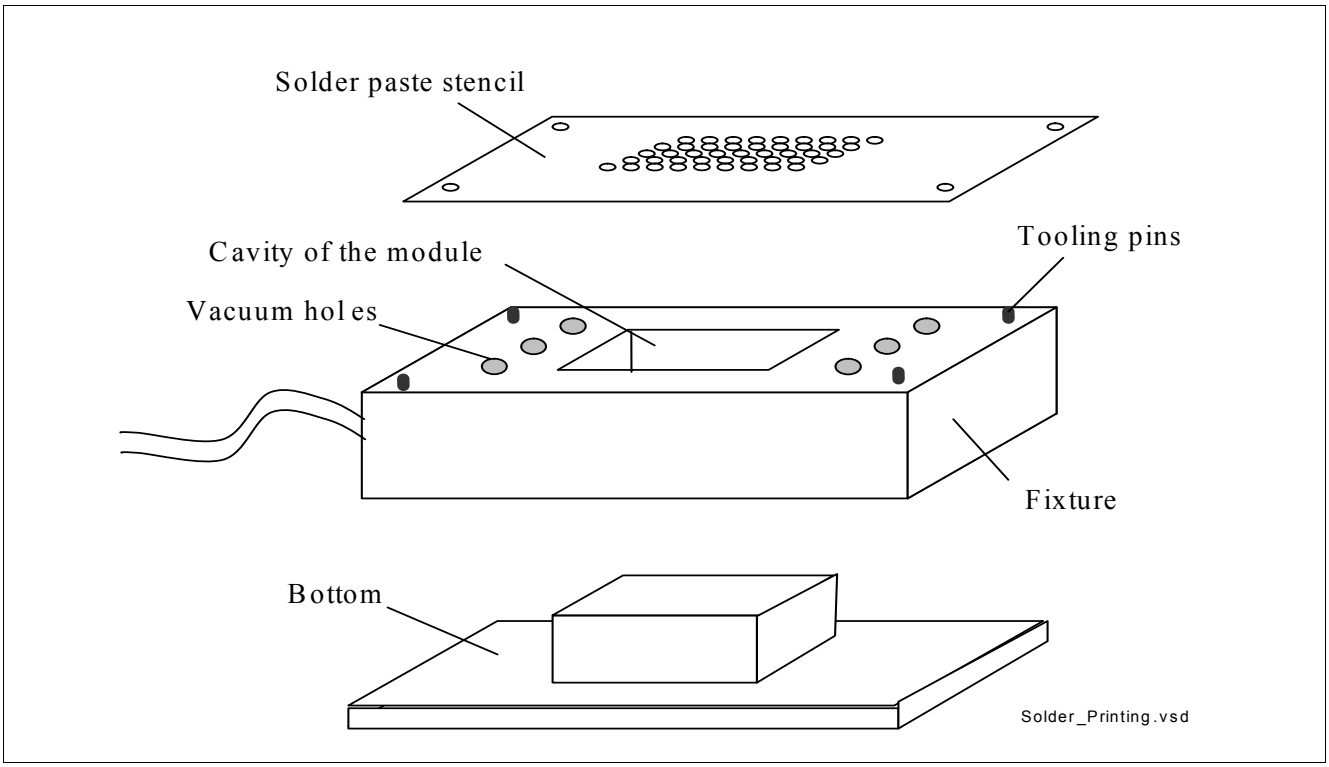


Figure 13 Solder Printing

1. Assemble the fixture to the bottom
2. Place the module in the cavity with the LGA pads upwards
3. Place the solder paste stencil on the fixture and make sure it fits to the tooling pins and the module
4. Apply vacuum to fix the solder paste stencil
5. Apply solder paste on the stencil and print by using a blade
6. Turn everything (bottom, fixture and stencil) upside down.
7. Separate carefully the bottom from the fixture
8. Pick the module by a nozzle and place in the right position on the board
9. Reflow the solder.

8.7 Inspection

Automatic inspection of the solder paste printing before assembly is highly recommended to ensure high yield and good long term reliability.

8.8 Component Salvage

If it is intended to send a defect PAN1321 module back to the supplier for failure analysis, please note that during the removal of this component no further defects must be introduced to the device, because this may hinder the failure analysis at the supplier. This includes ESD precautions, not to apply high mechanical force for component removal, and to prevent excess moisture content in the package during salvage (risk of pop corning failures). Therefore if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried 24h at 125°C before soldering off the defect component, because otherwise too much moisture may have been accumulated.

8.9 Voids in the Solder Joints

8.9.1 Expected Void Content and Reliability

The content of voids is larger on LGA modules than for modules with BGA or leads. At a LGA solder joint the outgassing flux has a longer way to the surface of the solder and it has a relatively small surface to the air.

The void content of the PAN1321 module conforms to IPC-A-610D (25% or less voiding area/area).

Figure 14 shows an example of void-content at a module assembled at production site. Normally you can see the whole spectra of void content variation within the same lot and occasion of assembly.

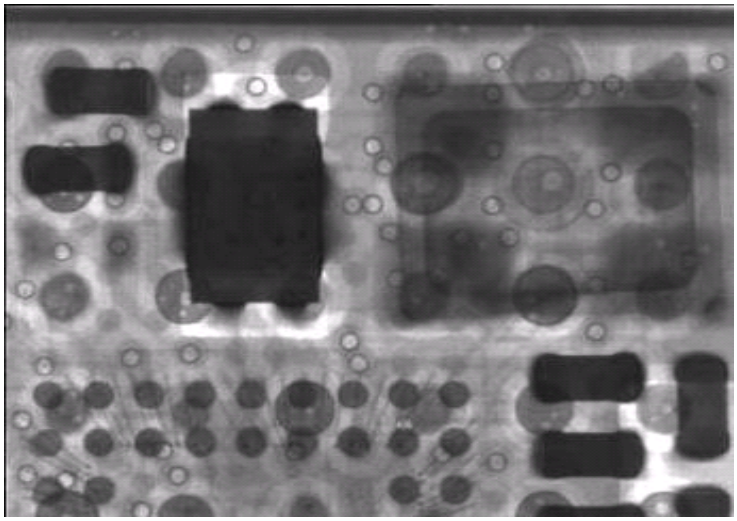


Figure 14 X-ray Picture Showing Voids Conforming to IPC-A-610D

8.9.2 Parameters with an Impact on Voiding

If the void content has to be reduced following parameters have an impact.

Solderability on module and PCB

Bad solderability is often connected to oxidation and has therefore a major impact on voiding. Flux will get entrapped on oxidized surfaces. In general, Ni/Au pads show fewer voids than HASL and OSP.

Solder paste

Higher activity of the flux will remove oxide rapidly and less flux will get entrapped.

Voiding increases with increasing solder paste exposure time, since long exposure time will result in more oxidation and moisture pickup.

Pad size

A large soldering pad means that the outgassing flux has a longer way to the surface of the solder, and will thereby create more voids.

Solder paste

Smaller powder size and higher metal load means more metal surface to deoxidize and thereby more entrapped flux and voiding. Higher metal load does also mean higher viscosity and more difficult for outgassed flux to remove from the solder.

Stencil thickness

A thick solder paste stencil means more surface area to the air and thereby easier for the outgassing flux to leave the solder.

Temperature soldering profile

Too short preheat time means that the flux does not get enough time to react and flux get entrapped in the solder and create voids.

Too long reflow time gives larger voids

Too short reflow time gives a fraction of voids

Terminology

A

ACK	Acknowledgement
ARQ	Automatic Repeat reQuest

B

b	bit/bits (e.g. kb/s)
B	Byte/Bytes (e.g. kB/s)
BALUN	BALanced UNbalanced
BD_ADDR	Bluetooth Device Address
BER	Bit Error Rate
BMU	BlueMoon Universal
BOM	Bill Of Material
BT	Bluetooth
BW	Bandwidth

C

CMOS	Complementary Metal Oxide Semiconductor
COD	Class Of Device
CODEC	COder/DECoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CTS	Clear To Send (UART flow control signal)
CVSD	Continuous Variable Slope Delta (modulation)
CDCT	Clock Drift Compensation Task
CQDDR	Channel Quality Driven Data Rate

D

DC	Direct Current
DDC	Device Data Control
DM	Data Medium-Rate (packet type)
DMA	Direct Memory Access
DH	Data High-Rate (packet type)
DPSK	Differential Phase Shift Keying (modulation)
DQPSK	Differential Quaternary Phase Shift Keying (modulation)
DSP	Digital Signal Processor
DUT	Device Under Test

E

EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory

eSCO	Extended Synchronous Connection-Oriented (logical transport)
EV	Extended Voice (packet type)
F	
FEC	Forward Error Correction
FHS	Frequency Hop Synchronization (packet)
FIFO	First In First Out (buffer)
FM	Frequency Modulation
FW	Firmware
G	
GFSK	Gaussian Frequency Shift Keying (modulation)
GPIO	General Purpose Input/Output
GSM	Global System for Mobile communication
H	
HCI	Host Controller Interface
HCI+	Infineon Specific HCI command set
HEC	Header Error Check
HV	High quality Voice (packet type)
HW	Hardware
I	
I2C	Inter-IC Control (bus)
I2S	Inter-IC Sound (bus)
IAC	Inquiry Access Code
ID	IDentifier
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
ISM	Industrial Scientific & Medical (frequency band)
J	
JTAG	Joint Test Action Group
L	
LAN	Local Area Network
LAP	Lower Address Part
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LO	Local Oscillator
LPM	Low Power Mode(s)
LPO	Low Power Oscillator
LSB	Least Significant Bit/Byte
LT_ADDR	Logical Transport Address
M	

MSB	Most Significant Bit/Byte
MSRS	Master-Slave Role Switch
N	
NC	No Connection
NOP	No OPeration
NVM	Non-Volatile Memory
O	
OCF	Opcode Command Field
OGF	Opcode Group Field
P	
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Coded Modulation
PDU	Protocol Data Unit
PER	Packet Error Rate
PIN	Personal Identification Number
PLC	Packet Loss Concealment
PLL	Phase Locked Loop
PMU	Power Management Unit
POR	Power-On Reset
PTA	Packet Traffic Arbitration
PTT	Packet Type Table
Q	
QoS	Quality Of Service
R	
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send (UART flow control signal)
RX	Receive
RXD	Receive Data (UART signal)
S	
SCO	Synchronous Connection-Oriented (logical transport)
SIG	Special Interest Group (Bluetooth SIG)
SW	Software
SYRI	Synthesizer Reference Input
T	
TBD	To Be Determined
TCK	Test Clock (JTAG signal)

TDI	Test Data In (JTAG signal)
TDO	Test Data Out (JTAG signal)
TL	Transport Layer
TMS	Test Mode Select (JTAG signal)
TX	Transmit
TXD	Transmit Data (UART signal)
U	
UART	Universal Asynchronous Receiver & Transmitter
ULPM	Ultra Low Power Mode
V	
VCO	Voltage Controlled Oscillator
W	
WLAN	Wireless LAN (Local Area Network)

References

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